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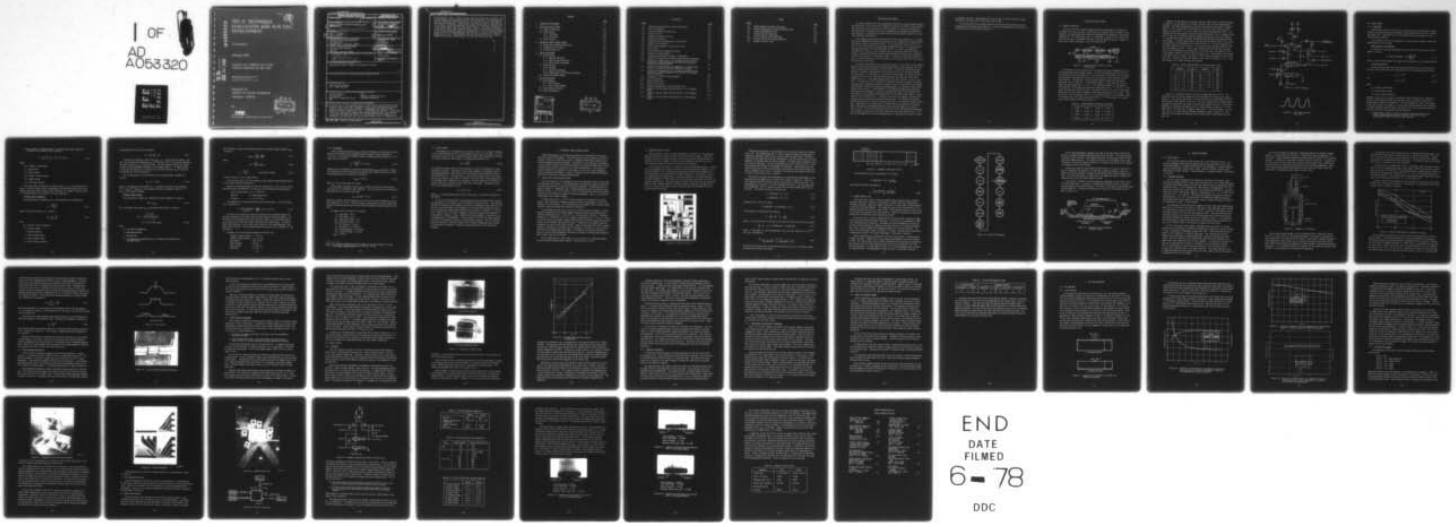

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The objectives of this program were to further advance the fabrication technology of small scale GaAs integrated circuits and to demonstrate the technology by fabricating and evaluating a 5 gigasample per second (Gs/sec) analog-to-digital converter bit cell. These objectives were met. In the TED/FET bit cell design the sampling and amplitude quantization are performed by a dual-gate TED under the control of a single-gate TED, the output bit is provided by the dual-gate TED, and the feed forward signal is generated by a

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FET differential pair. A total of only five active devices, including a FET current source, are required to perform these functions. The sampling rate actually achieved by the A/D cells was in excess of 8 Gs/sec, well beyond the 5 Gs/sec design goal. Additionally, the sampling rate is variable from 0 to 8 Gs/sec, unlike conventional A/D designs which generally operate only at one fixed sample rate, and well below 1 Gs/sec. The chief shortcoming of the A/D bit cells fabricated and tested under this program was inaccuracy of the feed forward gain, which was generally low. This is directly attributable to low FET transconductance, but pointed up the need for a means of adjusting cell gain. Some changes could also be made in the cell layout to improve port-to-port isolation, but this was not a critical item.

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1. INTRODUCTION AND SUMMARY

This report summarizes the work performed by TRW Defense and Space Systems between May 1976 and July 1977 on Contract No. N00014-76-C-0743 for the Office of Naval Research. The objectives of this program were to further advance the fabrication technology of small scale GaAs integrated circuits and to demonstrate the technology by fabricating and evaluating a 5 gigasample per second (Gs/sec) analog-to-digital converter bit cell. These objectives have been met.

This program started several months after, but was largely parallel to, a related ONR contract (N00014-76-C-0570) which produced the first combined GaAs transferred electron device (TED)/FET integrated circuits. It was not possible under this first contract to fully investigate all of the viable processing options, nor to develop any of the processing steps to a yield high enough for MSI or LSI levels of integration. Therefore two of the goals of this contract were to investigate additional processing options, including bulk resistors and an improved capacitor structure, and to generally increase the yield of all of the process steps. It cannot be claimed that yields are now at a level appropriate for LSI as a result of this program, but it will be seen that good progress has been made.

The TED/FET A/D converter bit cell which was used as a test vehicle in this program employs a unique design in which the threshold properties of gate controlled TED's are used in measuring the amplitude of an input signal. The overall A/D converter design approach is successive approximation, in which the first bit cell determines whether the input signal is in the upper or lower half of the A/D range; the second bit cell in conjunction with the first determines which quarter of the range; the third, which eighth, and so on. A more detailed description of the A/D operation is given in Section 2. Each bit cell in this A/D design is identical and must be capable of sampling its input signal, determining whether the sample is above or below the bit cell dynamic range midpoint, providing an output bit when appropriate, and providing a feed forward signal to the next cell. In the TED/FET bit cell design the sampling and amplitude quantization are performed by a dual-gate TED under the control of a single-gate TED, the output bit is provided by the dual-gate TED, and the feed forward signal is generated by a FET differential pair. A total of only five active devices, including a FET current source, are required to perform these functions. The sampling rate actually achieved by the A/D bit cells was in excess of 8 Gs/sec, well beyond the 5 Gs/sec design goal. Additionally, the sampling rate is variable from 0 to 8 Gs/sec, unlike conventional A/D designs which generally operate only at one fixed sample rate, and well below 1 Gs/sec. The chief shortcoming of the A/D bit cells fabricated and tested under this program was inaccuracy of the feed forward gain, which was generally low. This is directly attributable to low FET transconductance, but pointed up the need for a means

of adjusting cell gain. Some changes could also be made in the cell layout to improve port-to-port isolation, but this was not a critical item.

The sections which follow discuss the device and circuit design (Section 2), the integrated circuit process design (Section 3), the process development work (Section 4), and the A/D bit cell test results (Section 5).

2. DEVICE AND CIRCUIT DESIGN

2.1 THEORY OF OPERATION

The A/D cell and its required elements may best be understood in the context of the design for the A/D converter. While there are a number of ways to organize an A/D converter, the organization which takes best advantage of TED properties is the serial organization. This organization, which is illustrated in Figure 2-1, is also the most efficient in terms of the number of devices and the dc power consumption. However, it does require closer tolerances in the circuit fabrication.

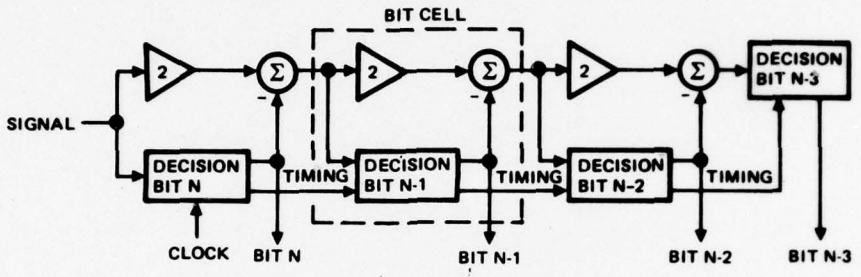

Figure 2-1. Successive Approximation or Serial A/D Converter

The purpose of the A/D converter is to provide a binary word representation of its input analog level at each sample instant. In the serial organization, the first bit cell provides the most significant bit of the output word, the second bit cell provides the second most significant bit, and so on to the last cell, which provides the least significant bit. Consider the listing of decimal numbers (range 0-15) and binary equivalents given in Table 2-1. If the decimal number is in the upper half of the range, the most significant bit is a "1". If the decimal number is in the second or fourth quarters of the range, the second most significant bit is a "1", and so on. The serial A/D works on the same principle. The output of each cell is a bit of the output binary word, the bits being of descending significance moving from left to right. Thus the first bit cell provides an output "1" if the analog signal is, at the sample instant, in the upper half of the range; the second provides a "1" if the signal is in the second or fourth quarter of the range, and so on.

Table 2-1. Decimal Numbers and Binary Equivalents

0-0000	4-0100	8-1000	12-1100
1-0001	5-0101	9-1001	13-1101
2-0010	6-0110	10-1010	14-1110
3-0011	7-0111	11-1011	15-1111

Suppose, for the purpose of an example, that the input signal to the A/D converter of Figure 2-1 can vary from 0 to 3.75 volts, and that 4-bit (16 level) quantization is required. The binary representation of each of the possible analog levels is shown in Table 2-2. Also suppose that at the moment the clock signal tells the A/D to take a sample, the input level is 1.4 volts, requiring a digital representation "0101". The decision bit N circuit examines the input to determine whether or not it exceeds 2 volts. Since it does not, the decision circuit provides no output pulse, that is, a digital "0", and the linear amplifier doubles the amplitude and provides the doubled amplitude to the summer. The other summer input is the decision bit output, either 0 or -4 volts. The summer takes the difference of 0 volt and 2.8 volts (2 x 1.4 volts) and feeds the 2.8 volts forward to the next bit cell. The next cell again determines whether or not its input exceeds 2.0 volts. Since it does, the decision circuit provides an output pulse, and the difference circuit subtracts 4 volts from the 5.6 volt amplifier input to the summer, leaving a 1.60 volt input to the next cell. The third bit cell provides a "0" output since its input is less than 2.0 volts, and feeds forward 3.2 volts to the final cell. The input to that cell exceeds 2 volts, and so its output is a "1". Thus, the required "0101" output code has been provided.

Table 2-2. Binary Representations of Possible Analog Levels

Voltage	Code	Voltage	Code
$0 < V < 0.25$	0000	$2.0 < V < 2.25$	1000
$2.25 < V < 0.50$	0001	$2.25 < V < 2.50$	1000
$0.50 < V < 0.75$	0010	$2.50 < V < 2.75$	1010
$0.75 < V < 1.0$	0011	$2.75 < V < 3.0$	1011
$1.0 < V < 1.25$	0100	$3.0 < V < 3.25$	1100
$1.25 < V < 1.5$	0101	$3.25 < V < 3.5$	1101
$1.50 < V < 1.75$	0110	$3.50 < V < 3.75$	1110
$1.75 < V < 2.0$	0111	$3.75 < V$	1111

Figure 2-2 illustrates the serial A/D cell designed under this contract. The operation of the cell may be compared to the block diagram of the basic cell shown in Figure 2-1. The input to the A/D cell is fed into one side of a differential FET pair which serves as the amplifier in the cell. The left FET amplifies the incoming signal and feeds it into the TED, T_B, which is the decision element of the cell. The decision element T_B is clocked by the output of the T_A. When the input to the cell is in the upper half of its range, T_B is triggered, generating a "1" at the bit output. (In this case, the "1" is a pulse from the TED whose waveform is shown in Figure 2-3.) The right FET sums the amplified input and the bit output which are fed forward into the next cell.

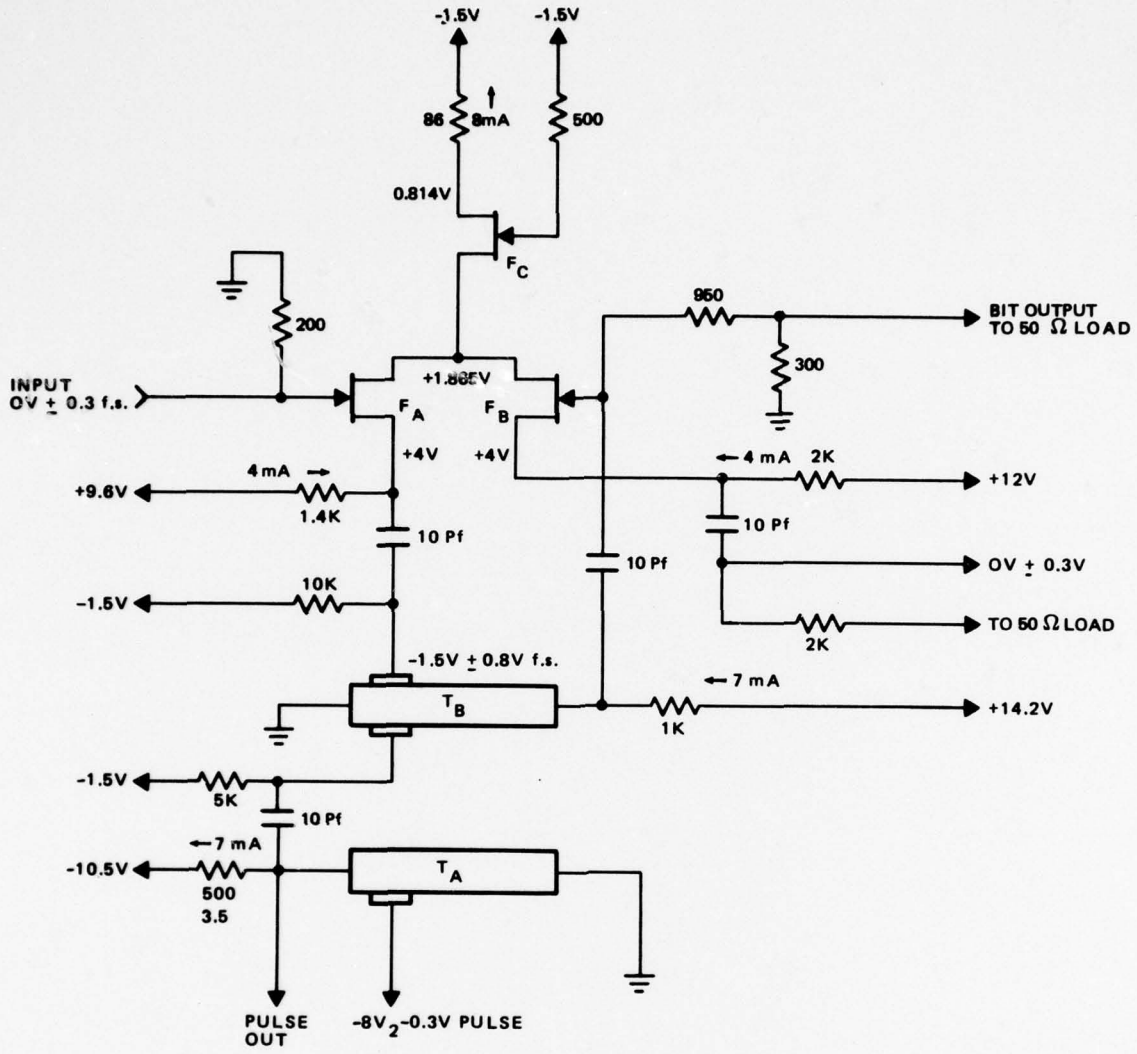

Figure 2-2. A/D Cell Schematic

Figure 2-3. Pulse Output Waveform from TED T_B

2.2 DEVICE DESIGN

2.2.1 TED Design

The dual-gate planar TED is basically a planar Gunn device with two ohmic contact terminals, called the anode and the cathode, and two Schottky barrier gates. The dual-gate planar TED is fabricated from an N-type GaAs epitaxial layer grown on a semi-insulating GaAs substrate.

In the design of a TED, the requirements of primary concern generally include the determination of the following.

Domain Transit Time Frequency

On the basis of previous measurements on 3 and 5 GHz TED's, the transit time frequency is given by

$$f = \frac{1.26 \times 10^7 \text{ cm/sec}}{\ell} \cdot \frac{\mu_m \text{ (measured)}}{8000} \tag{2.1}$$

where ℓ is the distance between the cathode and the anode and μ_m is the measured mobility.

EPI Section Criteria

The two conditions which have been determined experimentally to be necessary to achieve a large current drop after threshold occurs in a two-terminal planar TED are

$$n_o \ell_t \geq 10^{13} \tag{2.2}$$

and

$$n_o d \geq 10^{12} \tag{2.3}$$

where

n_o = electron concentration

ℓ_t = active channel length

d = active channel thickness

However, in the case of a three or four-terminal planar TED where gate triggering is desired, studies show that these two conditions are not necessarily sufficient for proper domain formation and propagation. With the placement of a gate in the channel of the TED, the built-in voltage, ϕ_L, and any applied gate potential cause a depletion in the epi thickness under the gate. This gives rise to the following two conditions that must also exist for gate-controlled TED operation:

- Before domain formation it must be possible to bias the portion of the channel outside the gate above the sustaining field level without exceeding the threshold field level under the gate

- Once a domain is formed the field in the channel must remain above the sustaining level and that field is given by

$$E = \frac{1}{\ell_{CA} - \ell_g - \ell_D} \left(V_a - V_D - E_g \ell_g\right) \tag{2.4}$$

where:

ℓ_{CA} = cathode to anode length

ℓ_g = gate length

ℓ_D = domain length

V_a = cathode to anode voltage

V_D = domain voltage

E_g = field under the gate

For minimum power dissipation and trigger voltage, n_o, ℓ_t, and d should be minimized. The active channel length is determined by the specified domain transit time frequency and should have a minimum length sufficient for a domain to build up after it is launched either at the cathode or at the trigger gate.

Threshold Power Consumption

The threshold power consumption P_o for a two-terminal TED is determined by

$$P_o = \frac{E_{th}^2 \ell_t^2}{R_o} \tag{2.5}$$

and the low field resistance, R_o, is equal to

$$R_o = \frac{1}{q\mu n_o} \frac{\ell_t}{wd} \tag{2.6}$$

where

E_{th} = electric field at threshold

q = electron charge

μ = electron mobility

w = active channel width

ℓ_t = active channel length

d = active channel thickness

By substituting (2.6) into (2.5) we obtain

$$P_o = q\mu n_o E_{th}^2 \ell_t wd \tag{2.7}$$

Therefore for minimum P_o, small values of n_o, ℓ_t, w, and d should be chosen. However, for satisfying the conditions $n_o \ell_t \geq 10^{13}$ and $n_o d \geq 10^{12}$ for a specified frequency, the lower limits for n_o, ℓ_t, and d are fixed. The only parameter that can be reduced to lower the threshold power consumption is the channel width, w. It should be borne in mind that the reduction of w increases the low field resistance, R_o, which may not be desirable for circuit applications.

For a three-terminal or four-terminal TED, the threshold power consumption is given by

$$P_{oG} = (1 - X)^2 P_o \tag{2.8}$$

where X is the depletion layer depth at Z = 0 divided by the active layer thickness, or $X = (\phi_d/\phi_p)^{1/2}$, where ϕ_d is the voltage drop across the depletion layer at Z = 0, and ϕ_p is the pinchoff voltage.

Minimum Trigger Voltage

The minimum input voltage, ΔVm, required for stable triggering is given by

$$\Delta Vm = \Delta_{min} \ell_t \tag{2.9}$$

for a two-terminal TED, where Δ_{min}, the minimum trigger field, is given by

$$\Delta_{min} = \frac{q^{3/4} n_o^{3/4}}{K^{3/2} \varepsilon^{5/4} (kT_e)^{1/4}}$$

$$\simeq 1.5 \times 10^{-10} n_o^{3/4} \text{ (V/cm)} \tag{2.10}$$

where

T_e = the electron temperature

k = Boltzmann constant

ε = permittivity

K = the dimensional fluctuation due to the thermal noise normalized to the Debye length

For a TED with a single or a dual-gate structure, the minimum trigger voltage, ΔV_{mG}, is equal to

$$\Delta V_{mG} = \frac{\Delta V_m}{\ell_t \, hgs} \, \frac{\Delta_{min}}{hgs} \tag{2.11}$$

where

$$hgs = \frac{\eta m_{th}}{2\phi} \, \frac{1}{X\,(1-X)} \tag{2.12}$$

$$\phi_p = \frac{q n_o \, d^2}{2\epsilon} \quad , \quad \text{the pinchoff voltage} \tag{2.13}$$

η and m are equal to 1 for a proper design.

As can be seen from (2.10), the reduction of the trigger voltage requires the use of low carrier concentration materials.

Based on the desired operation of the TED's and the FET's in this circuit, and on meeting the above considerations, the material for the TED design can be specified:

Doping concentration = $N_o = 2 \times 10^{16}$ cm^{-3}

Mobility = $\mu \approx 6200$ cm^2/volt-sec

Thickness = $d = 0.5 \times 10^{-4}$ cm

From equation (2.1) and the specifications of the epi-layer, ℓ can be calculated for a 5 GHz device as

$$\ell = \frac{1.26 \times 10^7 \text{ cm/sec}}{5 \times 10^9 \text{ Hz}} \cdot \frac{6200}{8000} = 19.53 \times 10^{-4} \text{ cm} \tag{2.14}$$

The width of the channel was chosen to provide the best compromise between the low power consumption of the device and sufficient width for good gate adhesion. The separation of the Schottky barrier gates from the cathode, ℓ_{cg}, and the gate length, ℓ_g, was minimized to reduce both power dissipation and trigger voltage. In choosing these minimum distances circuit yields and limitations of the photolithographic techniques were considered. The separation between the two gates is not important for this application.

In summary, the device design parameters for the TED's are:

Cathode to anode distance = ℓ = 19.5 μm
Cathode to gate distance = ℓ_{cg} = 5.0 μm
Gate length = ℓ_g = 5.0 μm
Gate separation = 4.0 μm
Channel width = w = 26.0 μm
Gate width = 11.0 μm

2.2.2 FET Design

With the doping concentration, N_o, and the epi thickness, d, specified by the TED design, the FET design may be completed using the grahpical design approach of R.B. Fair.* First the total pinchoff voltage, including the barrier potential of the gate, must be calculated

$$U_o = \frac{q N_o d^2}{2\varepsilon\varepsilon_o} = 4.1 \text{ volts} \tag{2.15}$$

Knowing U_o one may determine a saturated transconductance, $g_{m\,sat}$, from Fair's graphs. This value must be scaled according to the desired gate length, width, and an intrinsic transconductance factor yielding the relationship

$$g_{m\,sat} = 0.033\ Z_g \tag{2.16}$$

where Z_g is the FET gate width in microns.

With dc power conditions in mind, g_m was selected to provide the required gain for the A/D cell at reasonable load resistances. Given a desired g_m of 4 millimhos the gate width for the FET may be calculated

$$Z_g = g_m/0.033 = 121\ \mu m \tag{2.17}$$

From Fair's equation (25) and Figures 4 and 5, the drain-to-source saturation current was estimated to be 11.2 mA. The gate-to-source, gate-to-drain, and gate lengths were selected to maximize device yield while maintaining adequate frequency response in the FET's.

In summary, the FET's design is as follows:

Z_g = gate width = 121 μm
L_g = gate length = 3 μm
L_{gs} = gate-source length = 3 μm
L_{gD} = gate-drain length = 3 μm
d = epi thickness = 0.5 μm
N_o = epi doping = $2 \times 10^{16}/cm^3$
g_m = transconductance = 4 millimhos
U_o = pinchoff voltage = 4.1 volts
I_{DSS} = 11.22 mA

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*R.B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FET's," IEEE Trans. Electron Devices, June 1974, pp. 357-362.

2.3 CIRCUIT DESIGN

The schematic for a single A/D cell is shown in Figure 2-2. As stated in Section 2.2.2, the differential pair FET's are designed to have a g_m of 4 millimhos. The left FET provides a gain of 2.67, increasing the input dynamic range from 300 mV at the A/D cell input to 800 mV at the TED gate, as determined by equation (2.18)

$$\text{Gain} = \frac{g_m R_L}{2} \tag{2.18}$$

The right FET provides a gain of 2.0 as required in an A/D cell designed for a feed-forward A/D converter. The output of TED T_B, when triggered, is designed to have an approximate amplitude of 300 mV which will be subtracted from the amplified input in the differential pair. The lower TED, T_A, also provides a 300 mV pulse to the lower gate of T_B, setting up T_B so that if the input to the other gate is more negative than the midrange value, a domain will be triggered. The exact setting of the midrange is readily controlled by adjusting the dc bias inputs to the gate. The outputs of the TED's may be approximated as follows

$$V_o = (I_{p-v})\ (R_L) \tag{2.19}$$

where I_{p-v} is the predicted peak-to-valley current and R_L is the load resistance for the device.

All of the TED-TED and TED-FET interconnections are ac-coupled to permit individual adjustments of bias settings, and to avoid level shifting circuits. This makes the fabrication tolerances less stringent, facilitates experimentation with different bias settings, and avoids adding to the complexity of an already fairly ambitious circuit. The ac coupling does impose some constraints on the A/D cell's operation. An A/D cell with a sampling rate of 5 Gs/sec is capable of digitizing signals whose bandwidth is, by the Nyquist criterion, 2.5 GHz. Normally the signal bandwidth is taken from dc to a frequency equal to the bandwidth. The ac coupling in this A/D cell design requires that the signal bandwidth be taken at a higher center frequency. This will not pose particular problems in practical systems, since instead of downconverting the signal to be digitized to baseband, it would be frequency-translated to the center band frequency.

3. INTEGRATED CIRCUIT PROCESS DESIGN

Several technologies to fabricate GaAs monolithic A/D integrated circuits have been under extensive development. These technologies include an epitaxial deposition process, a mesa device fabrication process, a repeatable metallization process, and passive component processing techniques. Additionally, it was necessary to implement a circuit layout technique for minimizing parasitic resistance and capacitance, as well as minimizing chip area to enhance circuit yield and performance. This section discusses the material requirements for active devices, the circuit layout parameters, and the planned process sequence. Section 4 discusses the actual process development necessary to achieve the assigned performance goals.

3.1 ACTIVE DEVICE DESIGN SPECIFICATIONS

The active devices in the integrated circuits were mesa TED's and FET's fabricated on N-type epitaxial material. The N-type material was deposited on epitaxial GaAs buffers which were grown on Cr doped semi-insulating substrates. The detailed design is given in Section 2. The design values of doping concentration (N) and epitaxial layer depth (D) of $ND = 1 \times 10^{12}$ cm^{-2} and $N\ell_t = 10^{13}$ cm^{-2} were selected to meet the empirical criteria for TED differential negative resistance performance. Here ℓ_t is the transit length between the cathode and anode.

A design value of $N = 2 \times 10^{16}$ cm^{-3} and an epitaxial layer depth of 0.5 μm was chosen. These values were considered optimum for TED's and acceptable for FET's after thinning in the FET regions. FET's fabricated with this material have a slightly higher pinchoff voltage than desired for optimum FET performance.

The TED dimensions were chosen to achieve a 5 GHz oscillation frequency. The frequency was established by the length between cathode and anode, using the empirically verified relationship that $f = 1.28 \times 10^7 \mu/\ell_t$, as discussed in Section 2. Therefore a mobility, μ, of 6200 cm^2 volt^{-1} sec^{-1} suggests a design value of $\ell_t = 19.5$ μ_m. At the time of the design, experimental evidence indicated that the transit length for practical devices was the distance from cathode to anode. (Theoretically the domains should be launched at the gate and the transit length ℓ_t taken as the distance from gate to anode.) The gate in the design is separated from the cathode by a distance of 5 μm to avoid an electrical short between gate and cathode. This potential for shorting existed as a result of the poor photolithographic resolution at the base of the mesa when photoalignment is made to the top of the mesa.

The FET dimensions are a gate length, ℓ_g, of 3 μm with a 3 μm separation between source and gate and between drain and gate. The gate width is 121 μm.

3.2 INTEGRATED CIRCUIT LAYOUT

The A/D converter circuit is shown schematically in Figure 2-2. The topological design of the circuits used a rationale for the layout which included: simplicity, minimum of parasitics, minimum area for high yield, and uniform FET and TED gate orientation for ease of alignment. The layout also included the following test units: active devices, contact resistance bars, and isolated capacitors.

As can be seen from Figure 3-1, parallel lines are avoided when possible. Critical lines are separated as far apart as possible to minimize capacitance between the lines. The high frequency lines are bounded by ground planes forming 50 ohm coplanar lines. The ground planes are separated from the center conductor by 1/2 the width of the center conductor and each ground plane is five times the width of the center conductor. The center conductor is 2 mils wide to facilitate bonding to the center strip with 1 mil spacings on either side. Each ground plane is 10 mils wide, which uses up considerable GaAs chip area. Whenever possible, the ground planes are made near the edge of the chip so a portion of the width of one of the ground planes could extend off the chip onto the ceramic substrates.

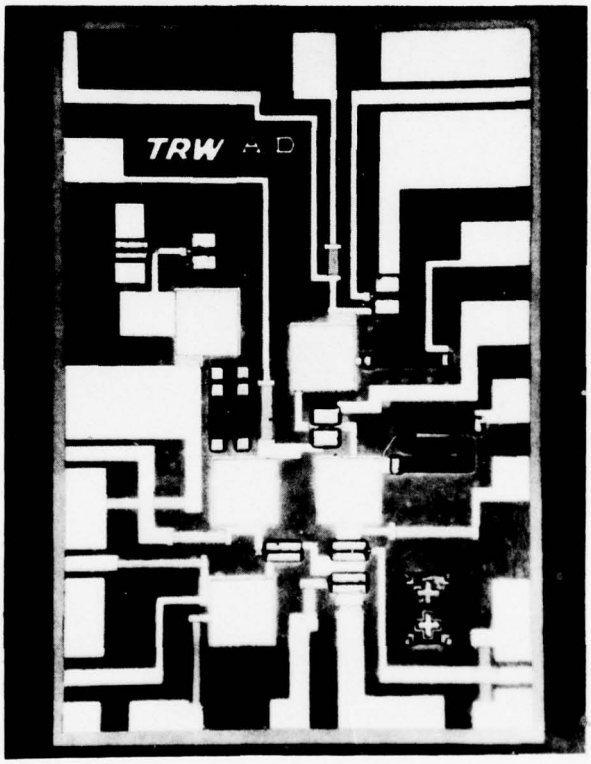


Figure 3-1. A/D Cell IC Chip

Minimizing chip area was a key consideration in the circuit layout for providing high yield. Since bonding pads are 3 x 4 mils minimum, the number of bonding pads is minimized by employing a power bus for circuits using the same voltage. The device location did not affect the chip area significantly, since the active devices are small compared to the bonding pads and passive elements. The largest passive elements on the chips are the capacitors. The size of the capacitors used in these circuits is larger than necessary but provides for two methods of fabrication. Test devices were also placed on the chips to allow characterization and testing of the devices without parasitics or damage to the circuits. A pattern of resistor bars was placed on each chip to allow for calculating contact resistance.

The contact resistance and the ND product are calculated from measurements of the resistance on each segment of the resistor bars as shown in Figure 3-2. There are three identical pads with identical contact resistance R_c on the resistor bars. They are separated by a distance, ℓ_ℓ, of 150 μm between pads 2 and 3. The resistance measured between pads 1 and 2 is called R_s, while the resistance between pads 2 and 3 is called R_ℓ. The contact resistance is derived from

$$R_\ell \text{ (measured)} = R_\ell + 2\,R_c \tag{3.1}$$

$$R_s \text{ (measured)} = R_s + 2\,R_c \tag{3.2}$$

Subtracting (3.1) from (3.2) gives

$$R_\ell \text{ (measured)} - R_s \text{ (measured)} = R_\ell - R_s \tag{3.3}$$

The ND product is derived from the relations

$$R_\ell = \rho \frac{\ell_\ell}{WD} \quad \text{and} \quad R_s = \frac{\rho\, \ell_s}{WD} \tag{3.4}$$

where ρ is the resistivity, W the width of the resistor, and D the epi layer thickness.

$$\frac{\rho}{WD}\,(\ell_\ell - \ell_s) = R_\ell \text{ (measured)} - R_s \text{ (measured)} \tag{3.5}$$

Since $\rho = 1/Nq\mu$ where N is the concentration, q the electronic charge of 1.6×10^{-19} Coul, and μ the mobility

$$ND = \frac{\ell_\ell - \ell_s}{\left(R_\ell \text{ (measured)} - R_s \text{ (measured)}\right) \times \mu W q} \tag{3.6}$$

This gives an excellent check on the material properties as well as providing a means for measuring the contact resistance.

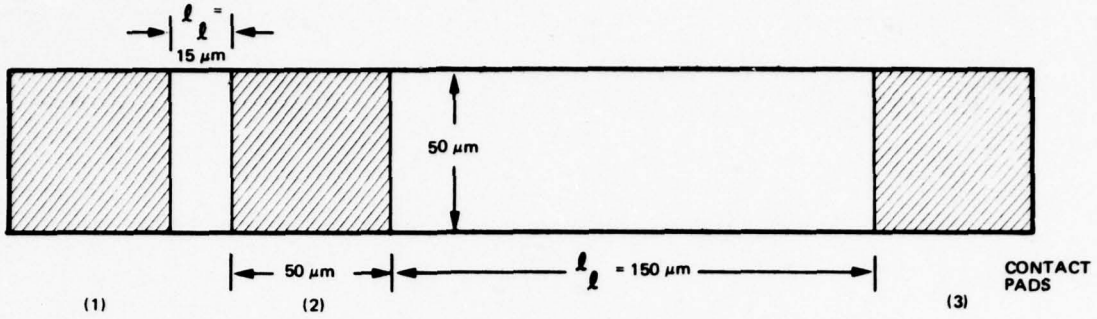


Figure 3-2. Schematic of Resistor Test Bar

The calculated ND value is substituted in (3.1) where

$$R_\ell \text{ (measured)} = 2\,R_c + \frac{\ell_\ell}{ND \times Wq\mu} \tag{3.7}$$

thus giving the contact resistance as

$$R_c = \frac{\left(R_\ell \text{ (measured)} - \frac{\ell_\ell}{ND \times Wq\mu}\right)}{2} \tag{3.8}$$

3.3 PLANNED PROCESS FLOW

The process flow, shown in Figure 3-3, begins with an epitaxial layer, with the parameters described in Section 3.1 deposited on a buffer layer over Cr doped semi-insulating substrate. Mesas are etched in the wafers to form islands of N-type material on the semi-insulating substrate. The islands are used to form isolated TED's, FET's, and bulk resistors when used in a given circuit. Bulk (GaAs) resistors are used in this circuit where the resistor values are noncritical. Mesas are etched using a photolithographic mask of AZ1350 and an H_2O: H_2SO_4: H_2O_2 etchant.

In the next step, an oxide is deposited over the entire wafer to prevent the GaAs from being etched during subsequent processing. The oxide is a low temperature 400°C silox, deposited using SiH_4 and O_2. The deposition time and temperature are kept low so that no adverse effects are produced on the GaAs surfaces or on device performance. This oxide is used throughout the processing sequence as a surface protectant. The oxide in the ohmic contact areas is patterned and etched. Then the ohmic contact metal is deposited and etched. The contact development is discussed in Section 4.

Several approaches were considered for the thin film resistors, including cermet, nichrome, and CrGe. Studies early in the processing development led to the selection of CrGe. The cermet process was not readily compatible with the GaAs device processing and nichrome films with small dimensions could not easily be controlled. The CrGe resistors employed in the fabrication of these circuits were developed under an internally funded program. The development of these resistors is discussed in Section 4.

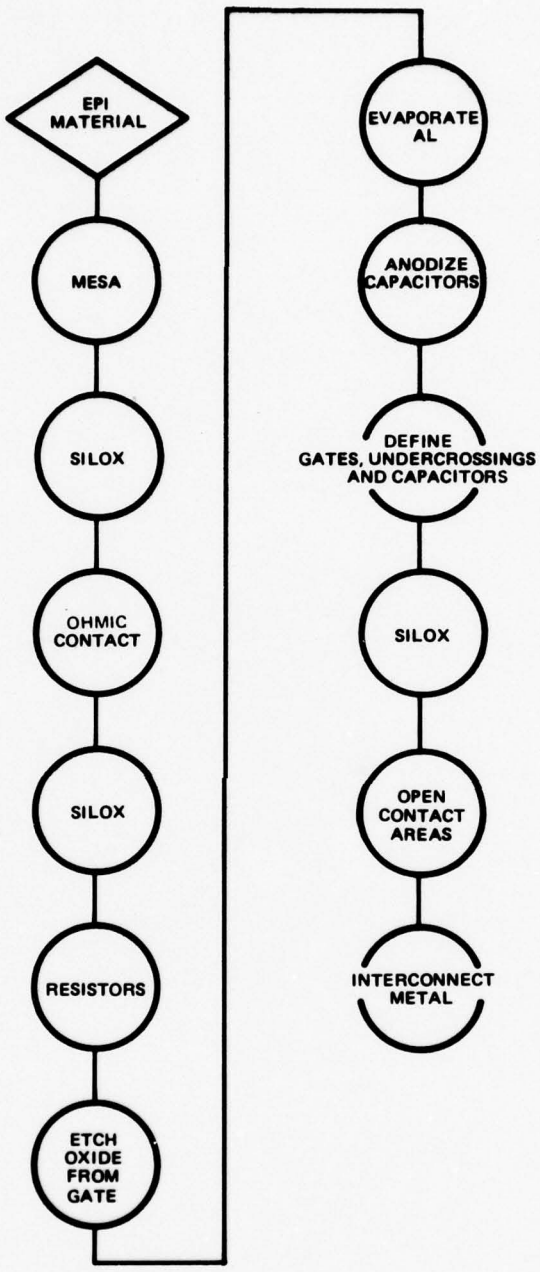


Figure 3-3. Process Flow Diagram

Using a photolithographic technique, the oxide in the gate region of the active devices is removed and aluminum evaporated over the entire wafer. This aluminum forms the gates for TED's and FET's, the undercrossing metal, and the bottom plate for metal-oxide-metal (MOM) capacitors. The capacitor areas are first delineated using a photolithographic mask and the capacitor dielectric is formed by anodization of the aluminum in an aqueous tartaric acid solution.

Aluminum was chosen for these metallizations because of its proven reliability in GaAs FET technology and because of its simplicity in device processing. After the capacitor plates are anodized, the gates are delineated using a photolithographic technique. The entire GaAs wafer is covered with a low temperature oxide to isolate the undercrossings, gates, and bottom capacitor plates.

Final contact is made to the active and passive components in the circuit using a TiAl interconnect metal. This metal is deposited by RF sputtering TiAl to achieve a strongly adhering low resistance contact. This metal is also used to form the top plate for the capacitors. A pictorial description of a section of the finished circuit is shown in Figure 3-4.

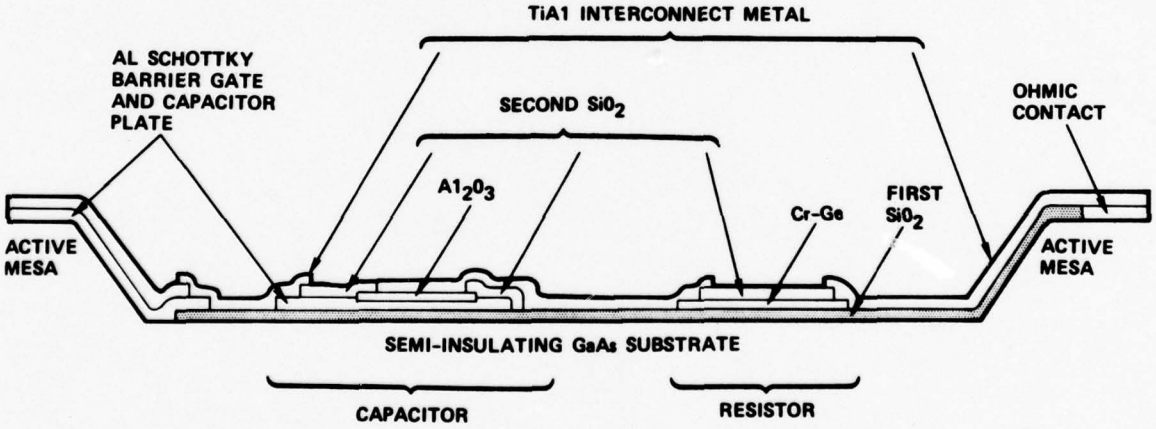


Figure 3-4. Compatible Passive Components for GaAs Circuits

4. PROCESS DEVELOPMENT

4.1 ACTIVE DEVICES

FET's and TED's were the active devices used in the integrated circuits. The primary development efforts were directed toward improving the design criteria and minimizing parasitics to achieve the desired circuit performance. The device development was concentrated in three specific areas: material selection criteria, gate fabrication, and ohmic contacts. This development is discussed in detail in the following sections.

4.1.1 Material Selection

The A/D circuits employed FET and TED devices fabricated in epitaxial layers deposited on buffered epitaxial layers rather than directly on the Cr doped substrates. It had been determined in earlier FET work that a buffer layer was required to minimize interfacial traps. In the development of a BPSK modulator and demodulator,[1] it was shown that a buffer layer is also required in fabricating precision TED's. The active layers for the TED's were N-type, doped to a concentration of $1.5 - 3 \times 10^{16}$ cm^{-3}, with a thickness of $1 - 0.5 \times 10^{-4}$ cm. These material parameters satisfied the empirical relationship $ND > 1.0 \times 10^{12}$ cm^2 required for TED differential negative resistance. The epitaxial material was thinned in the FET region to improve the quality of the FET. For optimum gain, an $ND^2 > 10^7$ was required.

The substrates on which the epitaxial buffer and active layers were deposited were doped with Cr to achieve a resistivity of 10^6 ohm-cm. These substrates were purchased to a specification of etch pit density of $<10^3$ cm^{-3}, resistivity $>10^6$ ohm-cm, surface with wafers sliced 3 to 5^o off the (100) toward the $\langle 110 \rangle$. The high resistivity semi-insulating properties are required for device performance while other specifications are chosen to enhance the surface quality of the epitaxial layers. It is uncertain at this point whether a higher dislocation density significantly affects either the surface of the epitaxial layer or the electrical properties of the devices.

Earlier investigators have reported a phenomenon where the surface of the substrates inverts and becomes P-type when the substrates are heated for a period of about 1/2 hour in hydrogen at temperatures greater than 700^oC. These conditions are quite similar to the conditions for epitaxial deposition. This inversion has not been observed in our laboratory, although precautionary screening techniques were established. With this screening it was observed that about 10% of one shipment lot of wafers had a high conductivity prior to heat treatment. In the earlier runs when this test was not made we aren't certain as to whether or not the inversion occurred. Even if it had existed, it may not have been noticed in our epi process since an in-situ etch is employed prior to epi layer deposition. The primary supplier of the Cr doped substrates was Crystal Specialities; the other suppliers could not respond in an acceptable time for this program.

The epitaxial deposition technology, although developed on an internally funded program, is presented here for continuity. The epitaxial layers are deposited in a vapor phase, vertical deposition system which employs AsH_3, Ga, and HCl as its principal reactants. A schematic of the epitaxial system is shown in Figure 4-1. It consists of a 5-zone furnace, a reactor tube, and a gas flow control system. Zone 1 preheats the entry gases and zone 2 maintains the Ga reservoir at the desired temperature. Zone 4 is the region where epitaxial layer deposition takes place, while zones 3 and 5 are buffer zones for temperature stabilization at zones 2 and 4.

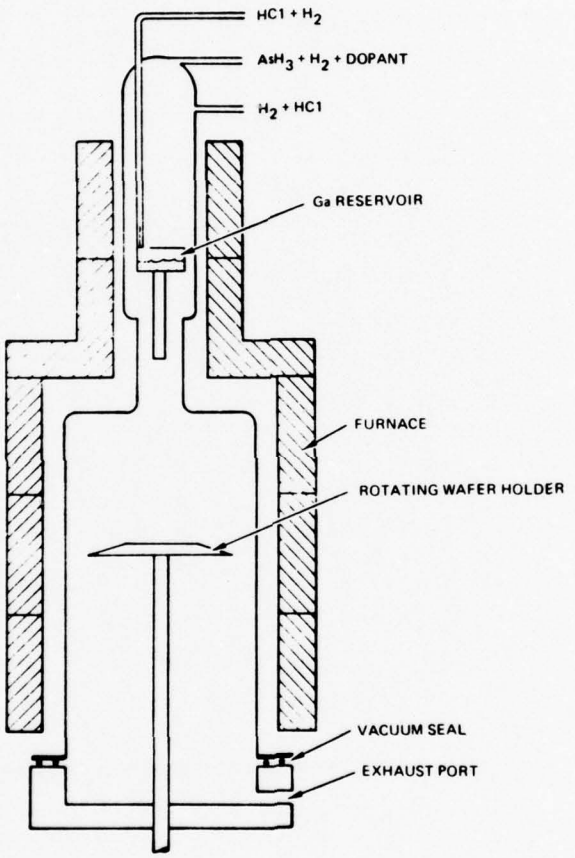


Figure 4-1. Schematic of EPI Reactor

The resistance heated furnace is split and operates with a "clam shell" motion. This aids in rapid cooling of the deposition chamber. The furnace is equipped with heat shields which cover each half of the furnace. These serve to establish an equilibrium temperature in the furnace prior to locking the two halves around the reactor tube, permitting the deposition chamber to be brought rapidly to the desired deposition temperature. This minimizes outdiffusion of dopants from the substrate during the time the wafer is being brought up to the deposition temperature.

The reaction tube has three entry ports for introducing the reaction gases. One port contains the Ga reservoir, through which HCl is passed to form GaCl. A second port is used for AsH_3 and H_2, and the third port is used for HCl and H_2 for etching and control of the background doping concentration. The deposited layers may be doped with sulfur by introducing H_2S at the second port.

By employing a high concentration of HCl in the reactor gases to reduce incorporation of silicon in the epitaxial layer, buffer layers of GaAs have been grown consistently at less than 10^{13} atoms cm^{-3} impurity concentration. Doped epitaxial films with free carrier concentrations ranging from 10^{15} - 2 x 10^{17} cm^{-3} have been prepared for different applications. This program used a semi-insulating buffer layer and an active layer with a doping concentration of 1.5 - 3 x 10^{16} atoms cm^{-3}.

Results of mobility measurements on epitaxial GaAs layers grown with and without buffer layers are compared in Figure 4-2. The reduction in compensation factor δ when a buffer layer is employed is apparent.

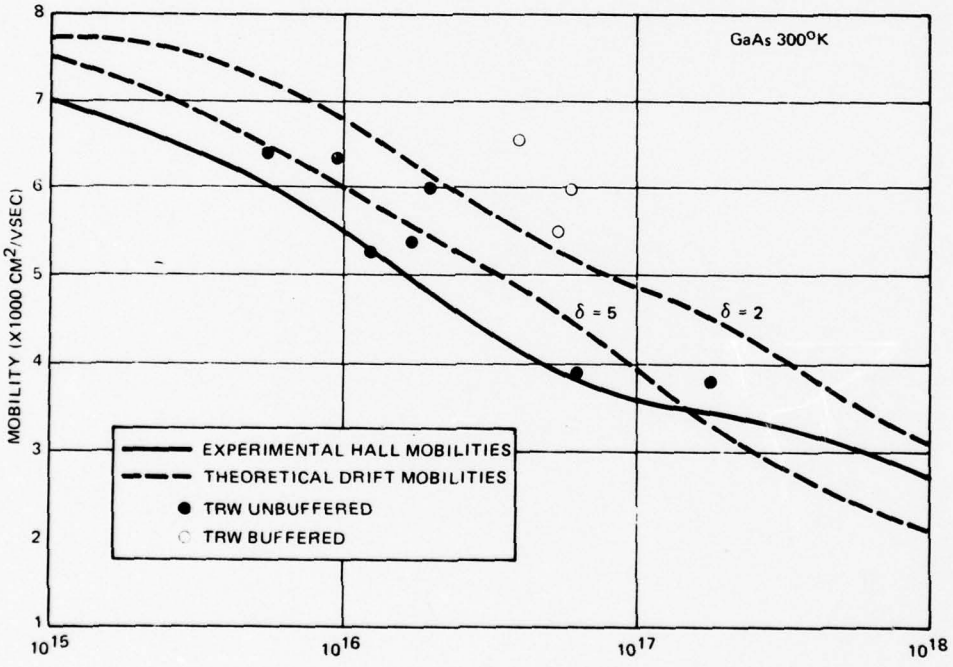


Figure 4-2. Mobility Measurements on Epitaxial Gas Layers

The concentration and depth of the active layers were measured and verified by several methods. The depth was measured by a groove and chemical stain technique. The groove and chemical staining technique for measuring the active layers correlates well with other measurement techniques if a buffer layer is used between the substrate and active layer. Without the buffer layer, the depth measured by the two techniques may vary as much as 75%. This variation is related to an inability to stain and measure the N/N+ layer accurately when the transition region is large. The varying width

of the transition region may be attributed to several conditions which include variations in Cr in the substrates and variation in the epi growth parameters. The cause of the transition region variation was not studied but the width of the region was minimized with the use of a nondoped semi-insulating buffer layer. Determination of the D and N from C-V data is accurate with active layers on buffers as long as the pinchoff voltage of the material does not exceed the avalanche breakdown voltage of the Schottky diodes, before the epi depletion has spread to the buffer layer (or the pinchoff voltage is reached). In the capacitance-voltage measurement of a Schottky diode, the concentration is expressed as

$$N = \frac{C^3}{A^2 \varepsilon\varepsilon_o q} \times \frac{dV}{dC} \tag{4.1}$$

where the capacitance C is the average of two differential capacitance measurements, ε is the dielectric constant, ε_o the permittivity of free space, q the electronic charge, and A the diode area.

The variation of diode capacitance with applied voltage is used to determine the electrical thickness of the epitaxial layer. The depletion spreading is expressed as

$$W = \frac{\varepsilon\varepsilon_o A}{C} \tag{4.2}$$

The electrical depth is determined arbitrarily as the point where the doping concentration is reduced by a factor of 2. The C-V data is computed and plotted automatically on a profiler.

Further, the ND product is verified from the N value calculated in the Hall mobility measurements. This value is used only for verifying N and D since the absolute values are dependent upon knowing either N or D accurately from an independent measurement. Materials of several ranges with and without buffer layers between the substrate and epilayers were used for device and circuit fabrication.

4.1.2 Mesa and Gate Fabrication

The first step of the process sequence, after epitaxial deposition, is device isolation. The device isolation in these circuits is accomplished by mesa etch. The mesas are etched in a solution of $H_2SO_4 : H_2O_2 : H_2O$ in the ratios of 5:1:1 at room temperature. These mesas are etched at a rate of $\approx$2.0 μm per minute. It was observed that GaAs material grown in the (100) direction exhibits preferential etching of the (111) planes in the above etchant. The resultant mesa profile is shown in Figure 4-3.

Photolithographic patterns are used to delineate the mesas during this isolation etch. This pattern must be aligned to the proper plane $\langle 01\bar{1} \rangle$ to assure that the gate metal covers the mesa with a gradual slope. A typical mesa showing good gate coverage is shown in Figure 4-4. The depth of etch must be sufficient to go completely through

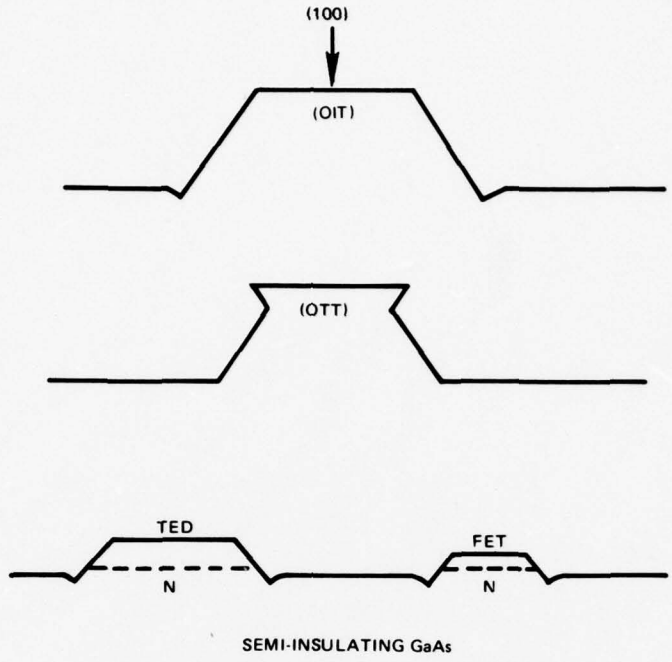


Figure 4-3. Mesa Profile

Figure 4-4. Typical Mesa Showing Good Gate Coverage

the active layer and approximately 0.5 to 1 μm through the buffer layer to assure device isolation.

If the FET area needs to be thinned, this is accomplished prior to the mesa etch by applying a photolithographic pattern which exposes the material in the FET region. This area is then etched in a more dilute mixture of $H_2SO_4 : H_2O_2 : H_2O$ which etches at a rate of ≈2000 Å/min.

There was no preferred sequence for forming the Schottky gates for gate quality. Schottky barriers by either sequence (gates before or after ohmic contact) gave sharp, low leakage device characteristics. However, if additional trimming of the FET channel is required, the ohmic contacts must be processed first in order to monitor the current as the GaAs is etched through the gate oxide mask opening prior to aluminum evaporation. The quality of the diodes was clearly a function of the cleaning technique and post deposition sinter conditions. A light clean of the gate region (with an oxide removel etch) and a sinter of about 10 minutes at 300°C was sufficient to achieve good diode characteristics.

4.1.3 Ohmic Contact Development

Ohmic contacts to GaAs have been extensively studied at TRW on an internally funded program and in other laboratories. The objective of these studies was to achieve metal semiconductor contacts which exhibit linear current-voltage characteristics and a contact resistance low in comparison to the resistance of the semiconductor device. This, in principle, is achieved either by:

- The choice of a metal which forms a low barrier with the semiconductor (thermionic emission)
- A high concentration region in the semiconductor near the contact so that the barrier is readily penetrated by quantum mechanical tunneling.

The tunneling approach was taken for the GaAs materials. In general, the objective was to reduce the specific contact resistance r_c to a value below 10^{-4} ohms-cm^2 by doping the semiconductor. This has been demonstrated in TRW's TED devices and in these circuits.

The low specific contact resistance was achieved by doping the GaAs with Ge from an AuGe contact. The Ge, an amphoteric dopant, goes substitutionally on vacant Ga sites to form donors. The doping occurs as the Au and Ge alloy with the topmost layer of the GaAs. When the GaAs-AuGe alloy solidifies, Ge is distributed in the GaAs regrowth layer. Contacts formed in this manner yield a low (≈10^{-4} ohm-cm^2) specific contact resistance.

The basic AuGe contact metallization has been used with and without variations in the structure. The variations included the use of additives such as Ag, In, Pt, and Ni to reduce the surface tension and minimize "balling" in the contact areas. For many of the early TED devices and the early circuit development, as shown in the process

flow, the AuGe contact was used with a simple coating of Au for bonding purposes. These contacts were not uniform throughout the contact area or across the wafer but had many islands of contact metal in the ohmic contact region. This caused the ohmic contact resistance to be higher than that achievable with a more uniform contact.

The nonuniformity was, in part, attributed to cleanliness of the wafer prior to metal deposition and to localized segregation of metal clusters due to the high surface tension of the metal. A cleaning technique which removed surface oxides was developed and employed during the circuit fabrication. This technique uses either dilute HCl or dilute NH_4OH to remove the oxides. The new cleaning procedure gave a higher yield of good contacts across a given wafer but the balling still existed. Balling was eliminated with the use of our present metal configuration and different sintering conditions.

Metals with various thicknesses of Au, Ge, Au (top metal), and Ni or Pt were investigated. The system of AuGe:Pt:PtAu was employed in the monolithic circuits developed on this program. Platinum was chosen over nichrome because Ni contacts give a high contact resistance, are more difficult to process, and exhibit some deterioration with age. The thickness of the metals used in the ohmic contact was: Ge, 200 Å; Au, 300 Å; Pt, 400 Å; Au, 3000 Å; and Pt, 400 Å. These contacts were deposited by E-beam evaporation and RF sputtering. It had been shown earlier that an optimum sinter temperature and time for the AuGe contacts was 450°C to 500°C for 2 to 5 minutes. Temperatures exceeding 500°C and times exceeding 5 minutes caused an increase in the specific contact resistance. Typical values of specific contact resistances achieved with this metallization system was on the order 10^{-4} ohm-cm^2 or less.

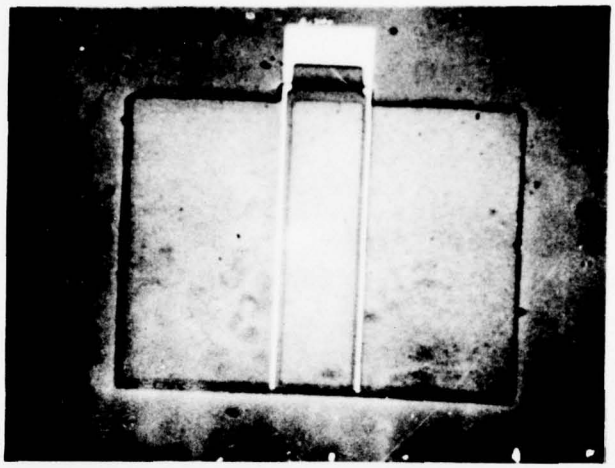
A comparison of the AuGe contact and the AuGe-PtAu is shown in Figure 4-5. It is clear that the ohmic contact balling is alleviated with the use of the Pt overlay. It was also felt that the Pt layer represents an excellent barrier between the AuGe contact and the topmost TiAl interconnect metal for future contact reliability.

4.2 PASSIVE DEVICES

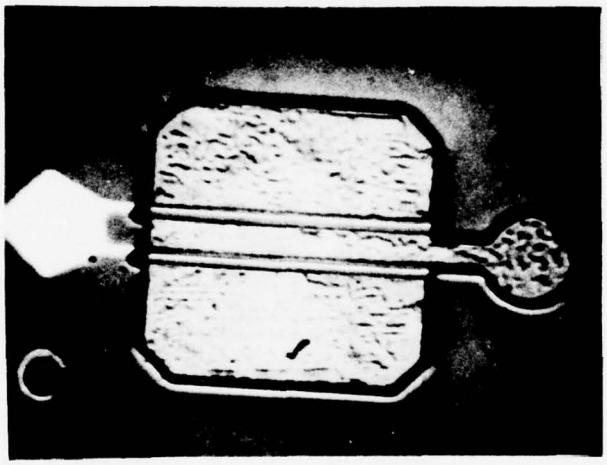
4.2.1 Resistors

Thin film resistors are used in the A/D circuit when the application requires a small value of resistance with high precision. These resistance values in the A/D circuit vary from 86 to 2000 ohms. Therefore a resistor material with a sheet resistance of 200 ohms/□ was chosen to achieve a minimum resistor area and ease of processing. Bulk resistors are used for the 5000 to 10,000 ohms required in the connections to the dual-gate TED.

Several materials were considered as candidates for fabricating the thin film resistors. These included nichrome, cermet, and CrGe. The chromium germanium material was chosen since it is the most stable of the materials, is compatible with GaAs processing, and is the best material for achieving the target resistor values. An equimolar mixture of CrGe is used for the resistors to give a final resistivity of approximately 1000 μohm-cm. During heating, the resistance value rises, but in a predictable manner. The contact resistance of this material is unaffected by low temperature oxide



a) With Platinum Overlay



b) Without Platinum Overlay

Figure 4-5. Comparison of AuGe Contacts

deposition. Low resistance contacts have been successfully made to this material with the TiAl interconnect metal.

After the material was selected and the deposition condition determined, a process for delineating the resistors was established. The resistor dimensions are defined using a negative photoresist and etched in a buffered ferricyanide solution. This etchant was developed specifically for the GaAs circuits.

Several methods of depositing the resistor materials were tried. These included E-beam evaporation, resistance heated boats, RF sputter deposition, and a resistance heated crucible. The vapor pressure curves (Figure 4-6) of chromium and germanium intersect at approximately 1300^{o}C. Therefore, if this temperature can be maintained

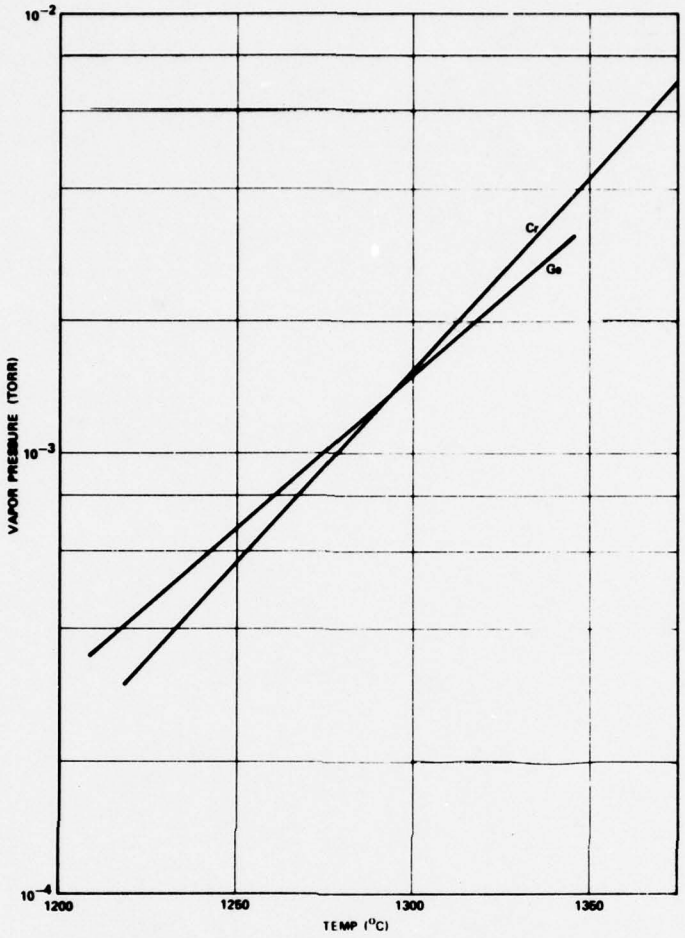


Figure 4-6. Chromium Germanium Vapor Pressure vs Temperature

throughout the evaporation run, the composition of the vapor and the melt will remain constant. Since previous work had indicated that the equimolar mixture should have a resistivity of 1000 μohm-cm, we started with this composition and tried to maintain a constant temperature of 1300°C. A glass bar 10 squares long (1 x 0.1 inch) was inserted into the chamber to monitor the resistance during the run. The wafer temperature was also monitored, but this proved to be an uncontrollable variable since radiant heaters were available only in the load lock area, and the block heater in the wafer holder heated each wafer differentially depending on the contact area.

Depositions using the E-gun were made while trying to follow a particular resistance vs time curve which had been found to give a good result. However, since the beam was not swept and the crucible in our system was very small, it was difficult to avoid hot spots in the melt. This caused an excess of chromium to be deposited even if the resistance was on target. Subsequent heat treatments had different and unpredictable effects on the resistivity depending on the actual resistor composition. The wafer and monitor bar resistances also differed so this method of deposition was abandoned.

Resistance heating was tried using molybdenum, tantalum, alumina coated boats, and finally tungsten boats. It was difficult to repeat constant temperature runs on any of the boats. In many cases the liquid melted through the boat. This even happened with the alumina coated boats. This susceptibility to run abortion at unknown times was undesirable. The tungsten boats appeared to give the most reproducible results but only when the deposit was ≈100 ohm/□ at the desired thickness. This was half of the value used in designing the circuits. Thinner, high sheet resistance deposits were very temperature sensitive. Since none of these runs gave predicatable, reproducible results, this method of evaporation was also abandoned.

Concurrent runs were made in a sputtering system using a mixed chromium-germanium target. This deposit acted differently from the evaporated mixture in that it did not etch in the same etch solution and had to be sputter etched. During temperature stabilization, the deposit also caused the underlying low temperature oxide to blister which left holes in the resistors. This effect was eliminated by using a sputtered oxide underneath the resistors, but the method still did not yield reproducible results. One IC run was made using this technique, but the resistance did not rise significantly during high temperature stabilization as anticipated from prior practice runs. Therefore, this resistor deposition method was abandoned.

At this time, an evaporation "furnace" was installed in the evaporator. This consists of a resistance heated alumina crucible with appropriate reflective shielding. There is a spring loaded thermocouple touching the bottom of the crucible to monitor the temperature. Initial runs were made while heating the substrates. This resulted in unpredictable resistivity variations between the glass monitor bar and the gallium arsenide wafers. This effect has been essentially eliminated by allowing the preheated wafers to cool to 60 to 70^{o}C prior to the evaporation. The monitor bar and the wafers now agree within 10%, and the resistivity rises approximately 150% during subsequent processing.

4.2.2 Capacitor Technology

A significant effort was made to fabricate capacitors for the A/D circuits with an acceptable yield. These capacitors are metal-oxide-metal capacitors where the metals are aluminum and the dielectric material is aluminum oxide. The capacitor yield was shown to be a function of the heat treatments following the fabrication of the metal plate and the dielectric material.

The capacitors were first made by anodizing a portion of the bottom aluminum plate and then using the interconnect metal for the top plate. These two metal layers are separated by the aluminum oxide. The aluminum used for the bottom capacitor plate is etched in other areas of the circuit to form the gates and undercrossings. Capacitances for these circuits should be 5 pF and matched within 2 to 3%. Alumina was chosen as a convenient dielectric material because aluminum gates were being evaporated anyway.

Since it has a higher dielectric constant than silicon dioxide, the capacitor size could be minimized.

The aluminum coated wafer is spun with photoresist, and the aluminum is exposed in the capacitor areas. Electrical contact is made to the edge of the wafer and a barrier layer of anodic aluminum oxide is grown in a 3% tartaric acid solution adjusted to a pH of 5.5. The aluminum is anodized to 120 volts which corresponds to an oxide thickness of 1560 Å. The capacitance of this layer is 0.323 pF/mil^2. At this time if a top metal plate is defined within the anodized areas, the capacitor yield is 100% on an area of 500 μm^2, thus indicating a pinhole density $<<1\ cm^{-2}$. However, when processing continues and the wafer is heated, degradation of the oxide is observed as the bottom aluminum apparently changes crystalline structure. This causes a high incidence of shorted capacitors. In order to reduce this effect the dielectric thickness had to be increased to ≈2500 Å. This added thickness improved the capacitor yield to approximately 95% from the 86% observed on the capacitors with the original thickness.

Further improvements in the yield were achieved by eliminating the thick gold-platinum layer on the ohmic contacts as previously discussed and by placing the capacitor formation after the ohmic contact.

4.2.3 Interconnects and Isolation Techniques

Most of the circuit elements are joined by the top metal; however, some connections through undercrossings are required in order to minimize the area and maintain a symmetrical layout. These connections are made with aluminum conductors which are deposited and defined along with the capacitor plate and gates. After this they are treated as one entity because they all must be protected by a deposited oxide and a hole must be etched into this oxide to permit contact to the top metal. This oxide also prevents the aluminum from reacting with the ohmic contact metals, particularly gold, and with the etches, some of which attack aluminum. The oxide is deposited by the oxidation of silane at 390°C. An RF sputter-deposited oxide could also be used if the system did not get excessively hot.

Titanium aluminum was chosen for the top metal because aluminum is easily bonded and etched while the titanium makes low resistance contacts to the resistors, bottom aluminum plates, gates, and the platinum on the ohmic contacts. The metal must be sputter deposited rather than evaporated in order to assure the low contact resistance required to the bottom aluminum. However, sputtered metal on oxide-coated GaAs wafers is often under such great stress that it rips holes in the oxide when the metal is removed during etching. Bias sputter deposition, that is, sputtering with a small negative bias on the substrate, reduces this stress. In addition, close control of the temperature of the aluminum etch solution has minimized this effect. The resultant metal stripes adhere to the oxide, but the metal is still sintered at 300°C to reduce the contact resistance to the underlying metals.

Following final test, the chips are separated by scribing and/or sawing. The sawing results in a ragged edge which is particularly bad in the [0$\bar{1}$1] direction. Therefore, this direction is usually scribed and broken. However, when it is desirable to have metal ground planes (for example, as close to the edge of the chip as possible) then the wafer has to be sawed. This can only be done in the "good" [01$\bar{1}$] direction where the minor chipping of the GaAs does not remove top metal.

4.3 PROCESS DEVELOPMENT SUMMARY

Several technologies have been combined in order to process this A/D integrated circuit. The ohmic contacts had to be uniform with a reasonably low specific contact resistance. Alloyed gold-germanium contacts to n-type gallium arsenide often exhibit poor wetting with resultant balling of the contact. This decreases the contact area and therefore increases the contact resistance. Such a contact would increase the observed threshold voltage and is undesirable in an integrated circuit. This problem was eliminated by ensuring that the gallium arsenide surface was properly cleaned prior to ohmic contact metal deposition and by the use of a top platinum layer to keep the underlying alloyed metal dispersed. The top platinum serves a twofold purpose since it also keeps the titanium separated from the gold. This ohmic contact system withstands repeated silox depositions without degradation of the contact. The gate diodes, which are the Schottky barrier type, initially presented a problem with excessive reverse leakage but this was also greatly reduced by proper wafer preparation before aluminum evaporation.

The thin film resistor process had to be perfected to enable us to predict final resistor values after various heat treatments. Thereafter, we could accurately select the desired initial sheet resistance readings. The final process yield is within an expected resistor tolerance.

The MOM capacitor yield was a major problem. Sputtering operations as well as the allcying temperature caused the aluminum to change structure thus ruining the integrity of the anodized layer. Increasing the dielectric thickness helped in preventing shorted capacitors.

The interconnect metal had some problems with open contacts to the bottom aluminum metal and adhesion of the underlying silox. Some minor processing changes appeared to eliminate these troubles.

Since the ohmic contact and gate yields are relatively high, the operation of the active devices is primarily dependent on the composition of the starting epitaxial GaAs. Therefore adequate evaluation of the material is essential. A dc circuit yield of 44% has been obtained as shown in Table 4-1.

Table 4-1. Circuit and Component Yields

Circuit Yield %		Component Yield %			
Calculated	Actual	Capacitors	Gates	TED or FET	Resistors
53	44	97	98	89	92

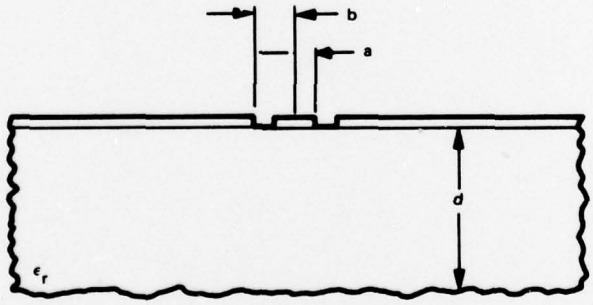
The lower yields in the TED or FET and the Resistor Columns in Table 4-1 were mainly due to low peak to valley ratios on the single-gate TED and an open contact to one of the bulk resistors. Since the single-gate TED depletes the entire channel width, it requires a slightly higher ND product than the dual-gate device to exhibit differential negative resistance. The bulk resistor yield was caused by an error in the interconnect metal mask where the metal crosses the sharp rather than the sloping mesa edge. The final circuit yield could be increased significantly by selecting slightly thicker epitaxial material and correcting the metal mask.

5. TEST AND EVALUATION

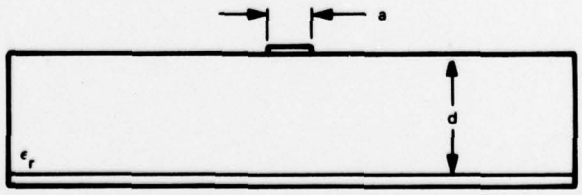
5.1 TEST EQUIPMENT

5.1.1 Test Fixtures

The transmission media used to test the A/D cell IC's was coplanar waveguide. Coplanar waveguide consists of a thin strip of plated metal on the surface of a dielectric slab with two plated metal ground planes running parallel to the strip on the same surface, as shown in Figure 5-1. If one assumes that the ground planes are infinitely long and the dielectric material infinitely thick, the characteristic impedance, Z_0, of the line is a function of the ratio a/b and the ε_r of the dielectric. For a given ε_r and a desired Z_0, the size of the center conductor of the coplanar line may be varied on the substrate without changing Z_0 as long as the ratio a/b remains constant. Naturally, an infinitely thick substrate and infinitely long ground planes can only be approximated. When a coplanar waveguide is placed in a container or mounted in a test fixture, the surrounding ground planes of the walls, top, and bottom of the fixture may be used to approximate an infinite ground plane on the substrate. The position of the sidewall top ground planes relative to the various transmission lines on the substrate has a minimal effect on the line impedance so long as they are far enough away from the transmission line.



a) COPLANAR WAVEGUIDE



b) MICROSTRIP WAVEGUIDE

Figure 5-1. Comparison of Geometries of Coplanar and Microstrip Waveguides

Investigation into this surrounding ground plane effect shows that the top and bottom ground plane positions effectively lower Z_0 when the planes come close enough to affect the field patterns between the center conductor and the parallel surface ground planes (Figure 5-2). Figure 5-3 shows that as the center conductor is made smaller, the effect of the fixture sidewalls on Z_0 become less.

To assure the position of the bottom ground plane in the fixture and to allow the connection of all the surface grounds for continuity, a bottom ground plane was added to the coplanar substrate design. Figure 5-4 shows the effect the top of the fixture has on Z_0 for a fixed bottom ground plane position. Note that the effect of this ground plane becomes negligible at a point greater than 0.030 inch above the transmission surface.

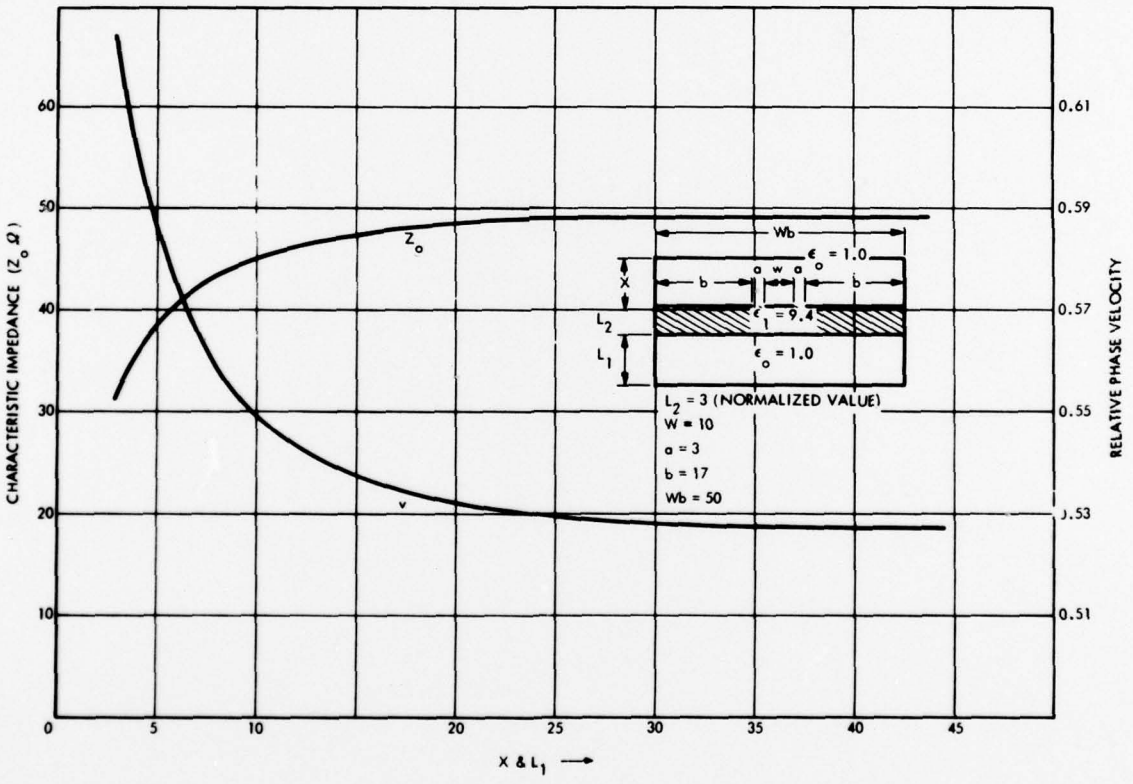


Figure 5-2. Variation in Characteristic Line Impedance and Relative Phase Velocity of a Coplanar Waveguide as a Function of Top-and-Bottom Ground Plane Position

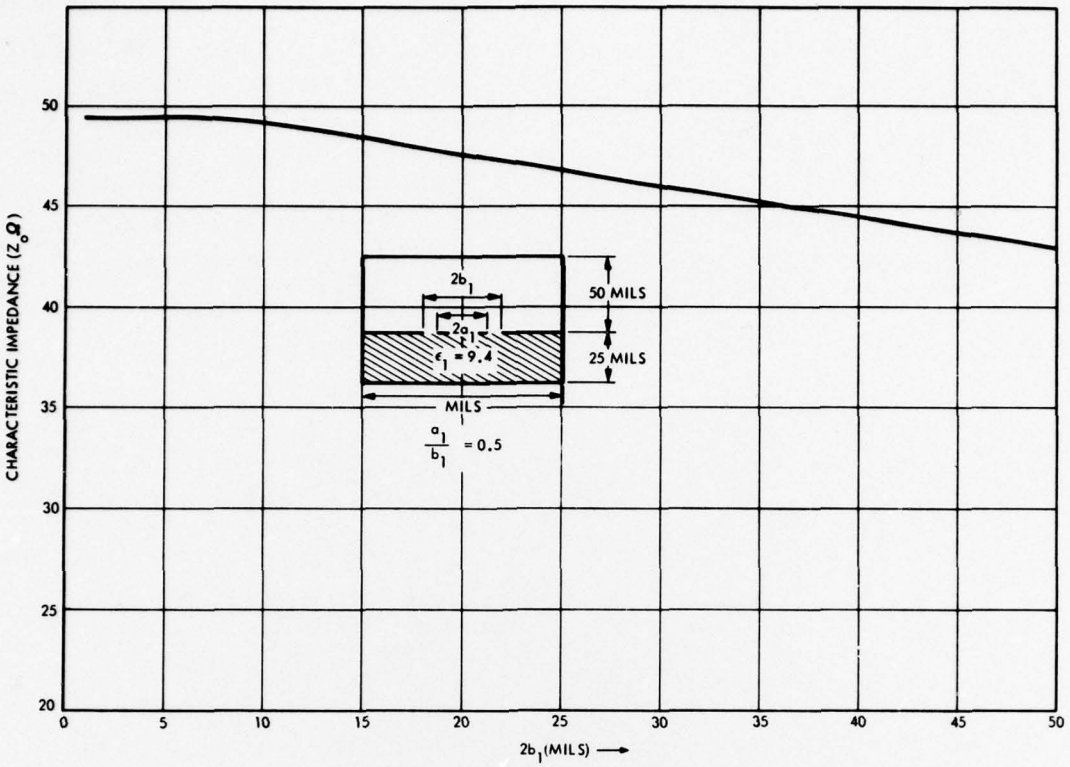


Figure 5-3. Variation in Characteristic Line Impedance of a Coplanar Wave-Guide as a Function of Side Wall Ground Plane Spacing

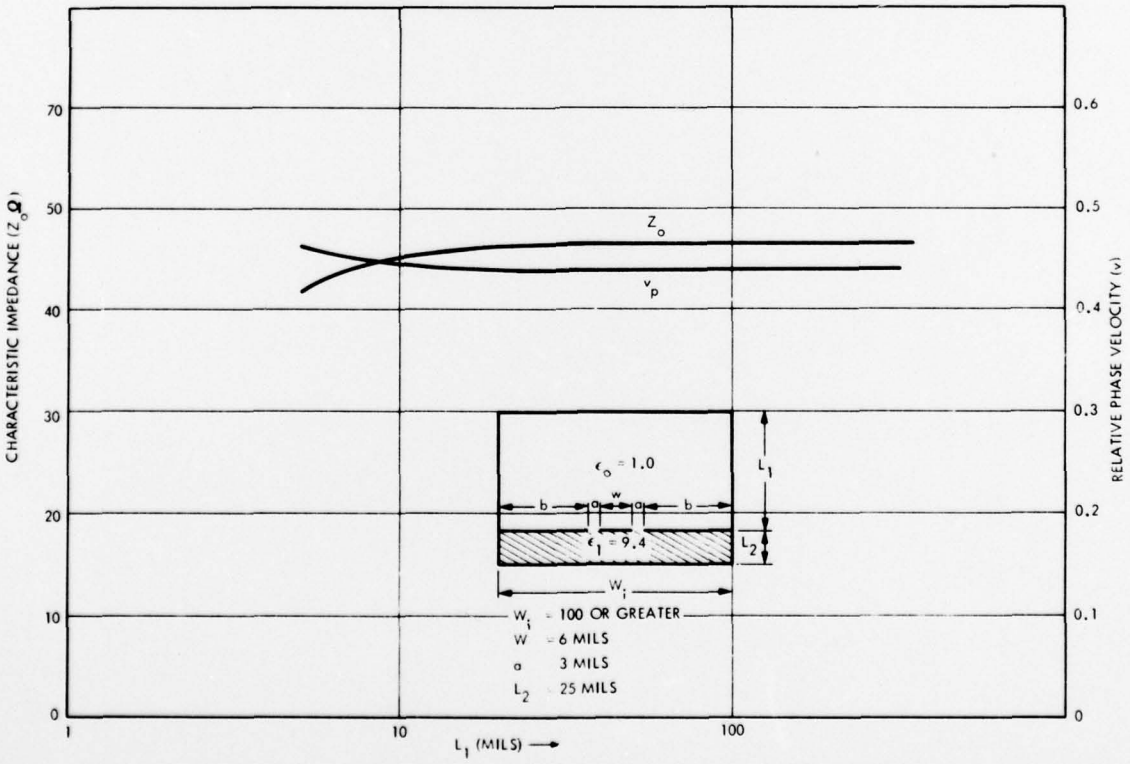


Figure 5-4. Variation of Characteristic Line Impedance and Relative Phase Velocity of a Coplanar Waveguide as a Function of Top Ground Plane Spacing Only

When more than one transmission line is plated on the dielectric, the isolation between the transmission lines is an important characteristic. The amount of isolation is proportional to the amount of ground plane between the two lines. To achieve a respectable 50 dB of isolation requires a ground plane distance of at least 5 times the width of the center conductor between the two adjacent lines. Since the center conductors used are small, the chip designer can have two or three transmission lines on one side of the IC chip with minimal cross-coupling between the lines. The impedance of the transmission lines used in the A/D cell test fixture is 50 ohms. The center conductor width varies from 20 mils at the connector interface to 2 mils at the chip-substrate interface.

The use of coplanar waveguide requires the IC chip surface to be in the same horizontal plane as the substrate surface so that the ground plane and center conductor interface with the chip is an continuous as possible. To satisfy this requirement and to simplify the mounting of the IC chip to the test fixture, the A/D cell substrates were made in two L-shaped configurations. The two halves fit together to form a rectangular shaped hole near the center of the substrate. A similarly designed fixture was constructed to accommodate the two substrate halves and provide a mounting pedestal for the IC chip and the connectors, as shown in Figure 5-5. The fixture was machined from brass and coated with a copper flash and an immersion gold finish. This design allows the IC chip to be properly aligned with the 2 mil coplanar lines on the surface of one-half of the substrate while it is being epoxied to the fixture. The other side of the chip can then be properly aligned with the other half of the substrate by placing the fixture halves together and adjusting the moveable side of the substrate until the 2 mil transmission lines are correctly aligned. The fixtures can then be bolted together, securing the alignment.

5.1.2 Test Fixture Assembly

The substrates used in these circuits are made of alumina with the following metallization:

200 A – NiCr
40 μin. – Au – vapor deposition
15 μin. – Au – strike (plate)
300 μin. – Cu – plate
54 μin. – Ni – plate
150 μin. – Au – plate

The copper plating allows the connectors to be soldered to the substrate. The Ni is a barrier to help prevent the surface Au and the Cu from alloying. Initially the alloying caused bonding problems at the chip and the Au surface was added to help provide the proper bonding surface. When the metallization is complete, the perimeters of the

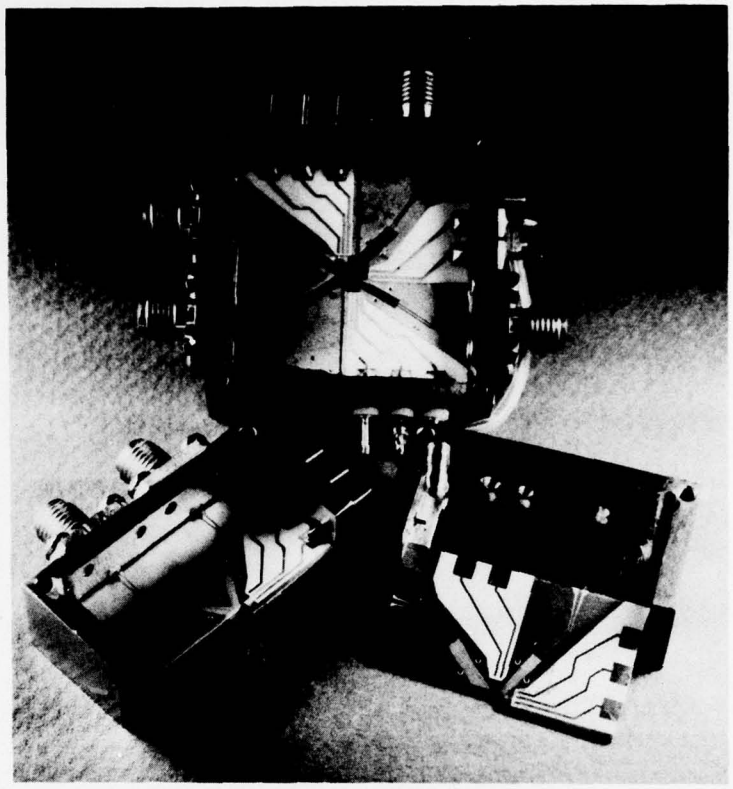


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Figure 5-5. Photograph of the Test Fixture Assembly

circuits are cut by a diamond saw on a horizontal cutting surface (Figure 5-6). The circuits are then cleaned and protected by plating tape.

The L-shaped portion has to be notched out of each half of the two substrates to form the rectangular hole for the IC chip. This is accomplished by placing the cutting surface perpendicular to the diamond blade and making several shallow cuts to the proper depth of the notch. After cutting, the circuits are degreased and cleaned in a J-100 solution to remove the cutting oil and tape gum from the surface. Each half of the circuit is then soldered into its respective fixture half. The external circuit connectors are soldered to their respective connector pads on the surface of the substrate. The fixture and the substrate are cleaned again to remove excess flux and oil in preparing the surface for bonding.

The IC chip is aligned to the 2 mil RF lines on the substrate, adjusted to its proper height through the use of shims, and epoxied into place on the appropriate fixture half. The epoxy is dried at 150^{o}C for 1-1/2 hours. The second half of the fixture is aligned to the 2 mil RF lines on the chip and the two fixture halves are bolted into place. Adjustments in the size of the hole required for the chip are made by sliding the two fixture halves to adjust one dimension and by adding shims between the fixture halves to adjust the other dimension.

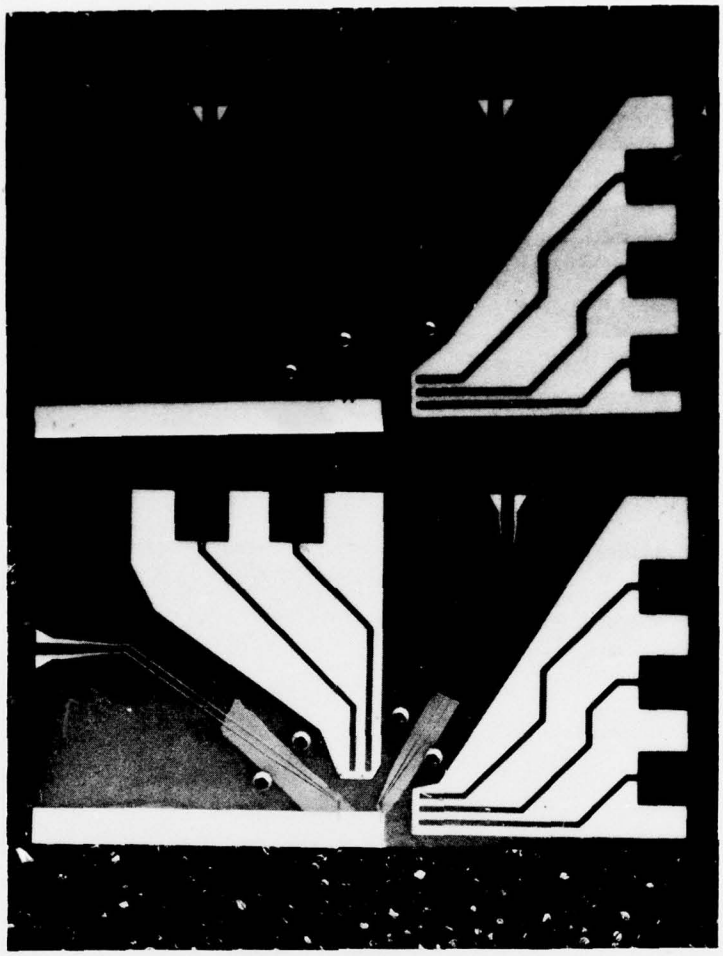

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Figure 5-6. A/D cell Substrate

Circuit connections are made by ultrasonic bonding 1 mil aluminum wire as shown in Figure 5-7.

5.2 TEST PROCEDURE AND SETUP

The test procedure for the A/D cell is fairly straightforward. The differential FET amplifier and the TED's are dc blocked to allow either group of devices to be biased first. Figure 5-8 illustrates the test configuration used to evaluate the A/D cell performance. Figure 5-9 is a schematic diagram that correlates the circuit bias points to those shown in Figure 5-8.

5.3 RESULTS AND ANALYSIS

The serial design of this A/D cell utilizes two basic building blocks: a FET differential amplifier, and a TED AND-gate used as a threshold detector. Even though these two circuit operations have been used before in previous circuit studies, the design of a serial A/D cell requires more stringent fabrication tolerance to achieve

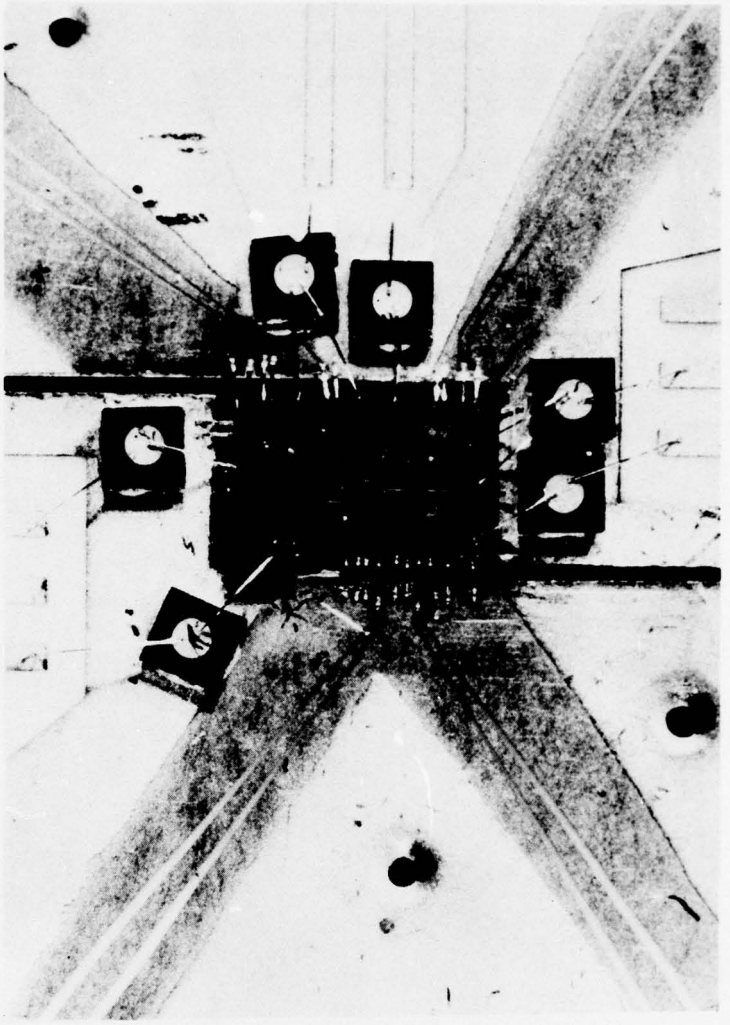

Figure 5-7. Bonded A/D Cell Chip

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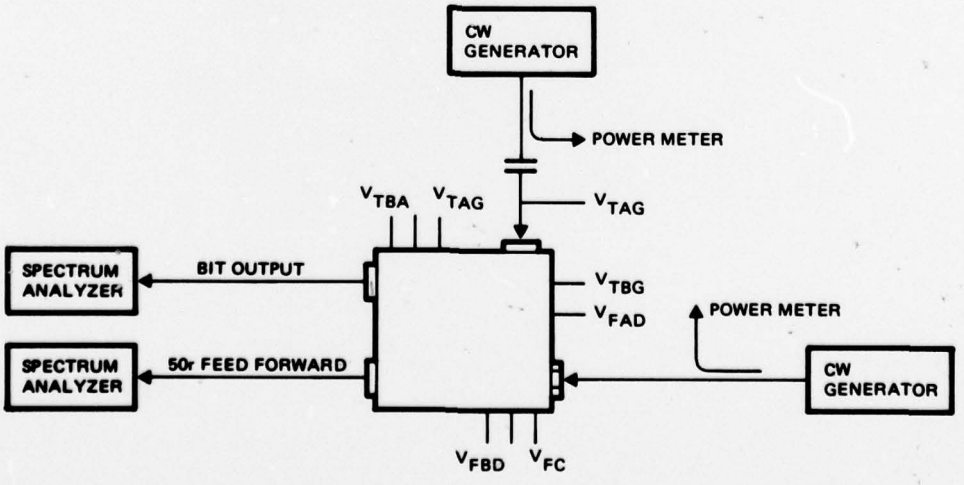


Figure 5-8. A/D Cell Test Set-Up

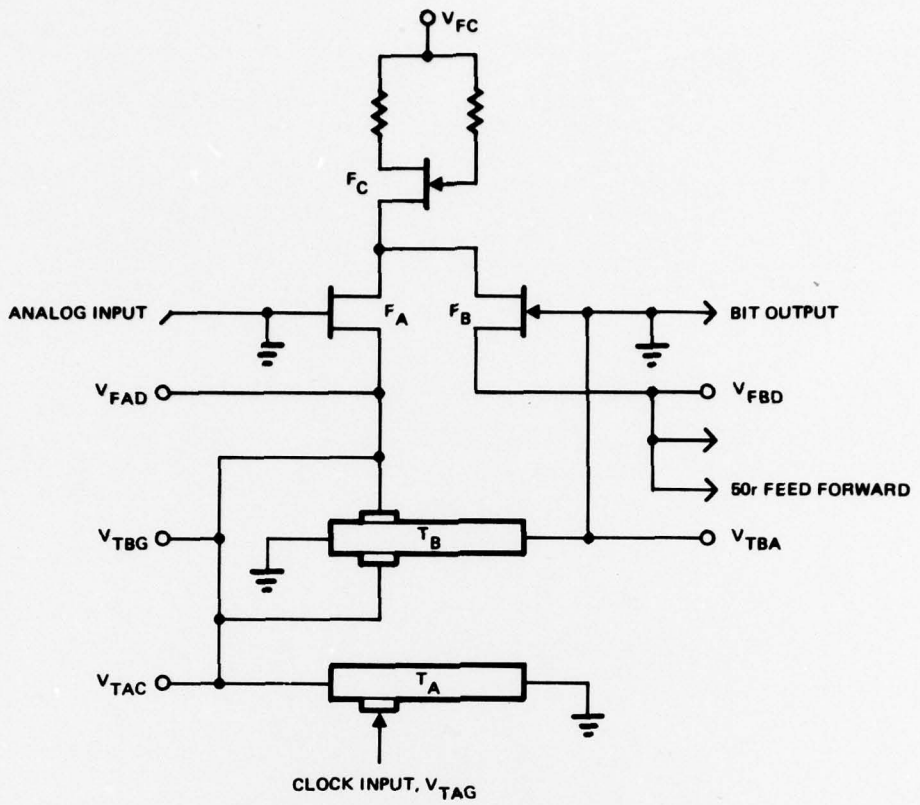


Figure 5-9. Schematic Showing Bias Points of A/D Cell Chip

the desired performance of the FET's and the TED's in the circuit. Table 5-1 compares the material design goals to the fabricated material characteristics. The fabrication process requires that the channels of FET's be etched to meet the desired I_{DSS} current. However, the process used to thin the FET channels causes uneven etching across the wafers. Tables 5-2 and 5-3 compare the design resistances and operating voltages to their typical measured values, respectively. As Table 5-2 shows, the values of both the bulk and the thin film resistors are higher than their designed values. This is due to two factors:

- During the thinning of the FET channels, the bulk resistors in the circuit were also slightly etched causing the resistor values to increase
- The thin film resistors were exposed to added heat processes, that were not anticipated in the original design, which raised their resistances slightly.

These changes in resistance values in the circuit do not have a major effect on the overall circuit operation.

The sampling process in the A/D circuit design is carried out by the FET, F_A, and TED, T_B, combination. The analog signal is fed into F_A which amplifies the signal that is fed to the gate T_B to be sampled. The FET differential pair and the TED's are dc

Table 5-1. A/D Cell Material Comparison

	Design	Actual
Material	GaAs	GaAs
Channel concentration (atoms/cm^3)	2.0×10^{16}	3.0×10^{16}
Channel thickness	0.5 μm	0.5 μm
Mobility	6200	5000

Table 5-2. A/D Cell Resistor Value Comparison

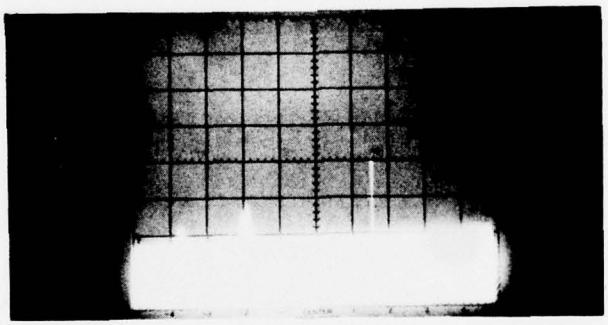
Type	Design (ohms)	Actual (Average ohms)
Bulk	10K	15K
	5K	7.2K
Thin film	2K	2.75 to 2.59K
	1K	1.33K
	950	1.20K
	500	626
	300	360
	200	226
	86	93

Table 5-3. A/D Cell Typical Bias Voltage Comparison

	Design	Actual
F_A drain voltage	+ 9.6 V	+ 9.6 V
F_B drain voltage	+12.0 V	+12.5 V
F_C source voltage	- 1.5 V	- 1.47 V
F_C gate voltage	- 1.5 V	- 1.47 V
T_A cathode voltage	-10.5 V	-15.6 V
T_A gate voltage	- 8.0 V	-11.5 V
T_B anode voltage	+14.2 V	+13.6 V
T_B gate voltage	- 1.5 V	- 2.7 V

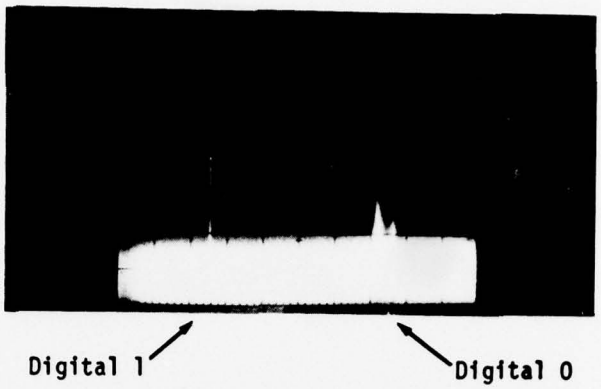
blocked by 10 pF capacitors. This simplifies the circuit design, but requires that the analog signal be translated up in frequency. This was simulated in the testing of the circuit by using a 3 GHz CW signal and varying its power as it was fed into FET F_A. The other gate of T_B receives the clock pulse from T_A. The output pulse from a TED provides a conveniently fast rise time, reducing the false triggering and hence reducing bit errors at the output of the cell. The maximum sampling rate in these circuits is 8 Gbps.

The digitizing of the analog signal takes place as follows. The triggering of T_B produces a pulse, after a small delay, at the bit output port of the cell. This takes place when the analog input signal rises above the midrange input level of the cell. The A/D cells tested had a midrange input level of about 0.0 dB. Figures 5-10, 5-11, and 5-12 show typical bit output data for the A/D cell. These figures are double exposed photographs showing the bit output when the analog input is less than and greater than the midrange input level of the cell. As discussed in Section 2, when the analog input is less than the midrange input level, the bit output is a digital zero. When the analog input is greater than the midrange level, the bit output is a digital "1". The digital "1" shown in these figures is actually a time average display of digital "1"s created by maintaining the analog input above the midrange level and sampling the signal at a rate of 7.8 to 8.1 Gbps.



Clock frequency: 8.08 GHz
Clock input power: -9.0 dBm
Analog frequency: 3.1 GHz
Midrange analog input level: 0.0 dBm

Figure 5-10. Example of the Bit Output from the A/D Cell in the Frequency Domain

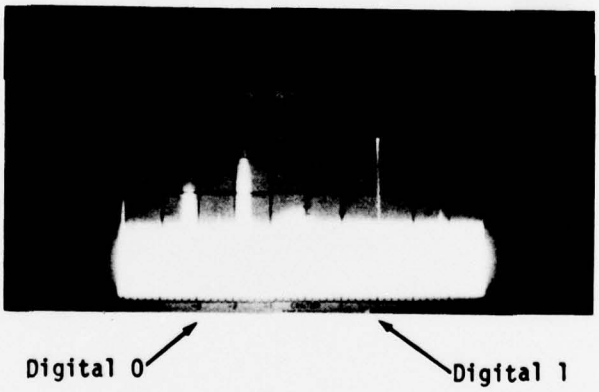


Clock frequency: 7.9 GHz
Clock input power: -2.3 dBm

Analog frequency: 3.1 GHz

Midrange analog input level: 0.0 dBm

Figure 5-11. Example of the Bit Output from the A/D Cell in the Frequency Domain



Clock frequency: 7.87 GHz
Clock input power: -6.0 dBm

Analog frequency: 3.1 GHz

Midrange analog input level: 0.0 dBm

Figure 5-12. Example of the Bit Output from the A/D Cell in the Frequency Domain

For a serial organization of A/D cells, the gain and summation operations of each cell are critical to the proper operation of a serial A/D converter. The summation and feedforward operation of this cell are accomplished in the FET differential pair. The FET pair amplifies the analog input by a factor of 2 and F_B provides the summation operation between the amplified input and the bit output pulse (when present). However, the nonuniform etching of the FET channels also contributes to a variation in the transconductance of the FET's across the wafers. The differential FET's in the cell were designed to have a g_m of 4 millimhos. However, the majority of the FET's that were tested had g_m's ranging from 2 to 3 millimhos.

To summarize, the A/D cell circuit samples an analog signal, digitizes that signal, and provides a feedforward signal to allow the cascading of single cells to form a multiple-bit A/D converter. Due to the reduced gain experienced in the FET differential amplifier, the desired feedforward amplitude was too low for optimum performance. However, the sampling and digitizing of the analog signal was accomplished with a notable increase in sampling rate over conventional designs. In addition to the obvious contrast in sampling rates between this A/D cell design and conventional designs, this design has the capability of varying its sampling rate from 0 to 8 gigasamples per second. Further, although the actual 330 mW dc power is slightly over the 300 mW design goal, it compared very favorably with the 1250 mW per bit of the best high speed silicon technology A/D converters. Table 5-4 summarizes the A/D cell data.

Table 5-4. Summary of A/D Cell Data

Parameter	Goal	Actual
Sample rate	0 to 5 Gs/sec	0 to 8.1 Gs/sec
Clock drive level	≤0 dBm	-6 dBm
Midrange input level	0 dBm	0 dBm
Analog input frequency	≥2.5 GHz	≥2.5 GHz
Feed forward gain	2	≤1
DC power	300 mW	330 mW

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